

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Dougherty et al.

Examiner: P. Dinh

Serial No: 10/780,140

Group Art Unit: 2825

Filed: February 17, 2004

Docket: YOR920030437US1
(8728-653)

For: METHOD FOR OPTIMIZATION OF LOGIC CIRCUITS FOR
ROUTABILITY IMPROVEMENT

Mail Stop AF
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RESPONSE

Sir:

This is a response to the Final Office Action dated November 20, 2007.

Reconsideration of the above-identified application is respectfully requested.

OK to enter
PD
1/22/08